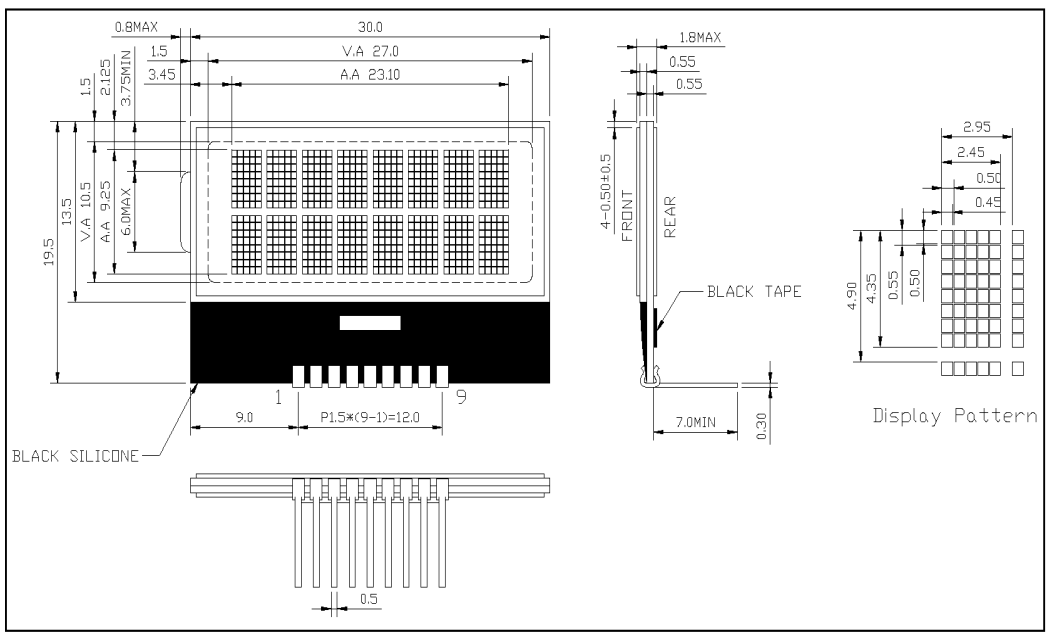
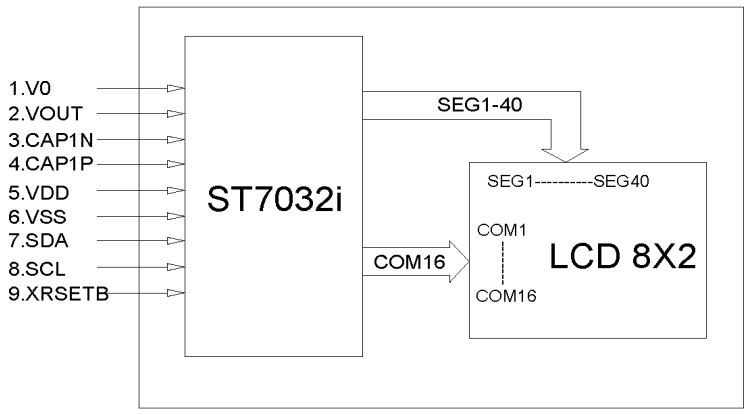
I2C接続小型8文字×2行液晶

AQM0802A-RN-GBW

★３０mm×１９．５mm（画面２７mm×１０．５mm）の超小型サイズです。
★マイコンとの接続は、信号線２本のＩ２Ｃインターフェイスです。
★液晶コントラストは、コマンドで設定しますので外付けＶＲが不要です。
★電源電圧３．３Ｖで、消費電流１mA



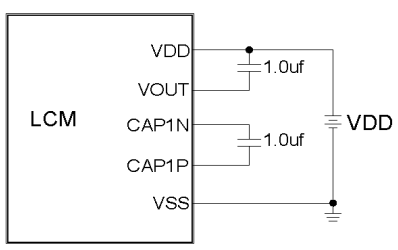
BLOCK DIAGRAM



PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VO	Test PIN for VLCD,leave it open
2	VOUT	DC/DC voltage converter output
3	CAPIN	For voltage booster circuit(VDD-VSS)
4	CAPIP	External capacitor about 0.1u~4.7uf
5	VDD	+3.3V
6	VSS	Ground
7	SDA	Serial data input
8	SCL	Serial clock input
9	XRSETB	Chip reset signal. Active when low

POWER SUPPLY



GENERAL SPECS

1. Display Format	8*2 Character
2. Power Supply	3.3V
3. Overall Module Size	30.0mm(W) x 19.5mm(H) x max 5.5mm(D)
1. Viewing Area(W*H)	27.0mm(W) x 10.5mm(H)
1. Dot Size (W*H)	0.45mm(W) x 0.50mm(H)
2. Dot Pitch (W*H)	0.50mm(W) x 0.55mm(H)
3. Character Size (W*H)	2.45mm(W) x 4.35mm(H)
4. Character Pitch (W*H)	2.95mm(W) x 4.90mm(H)
5. Viewing Direction	6:00 O'Clock
6. Driving Method	1/16Duty,1/5Bias
7. Controller IC	ST7032I-0D or compatible
1. Display Mode	STN(Gray)/Positive/Reflective
1. Backlight Options	NC
1. Operating temperature	-20ºC ~ 70ºC
1. Storage temperature	-30ºC ~ 80ºC
2. RoHS	RoHS Compliant

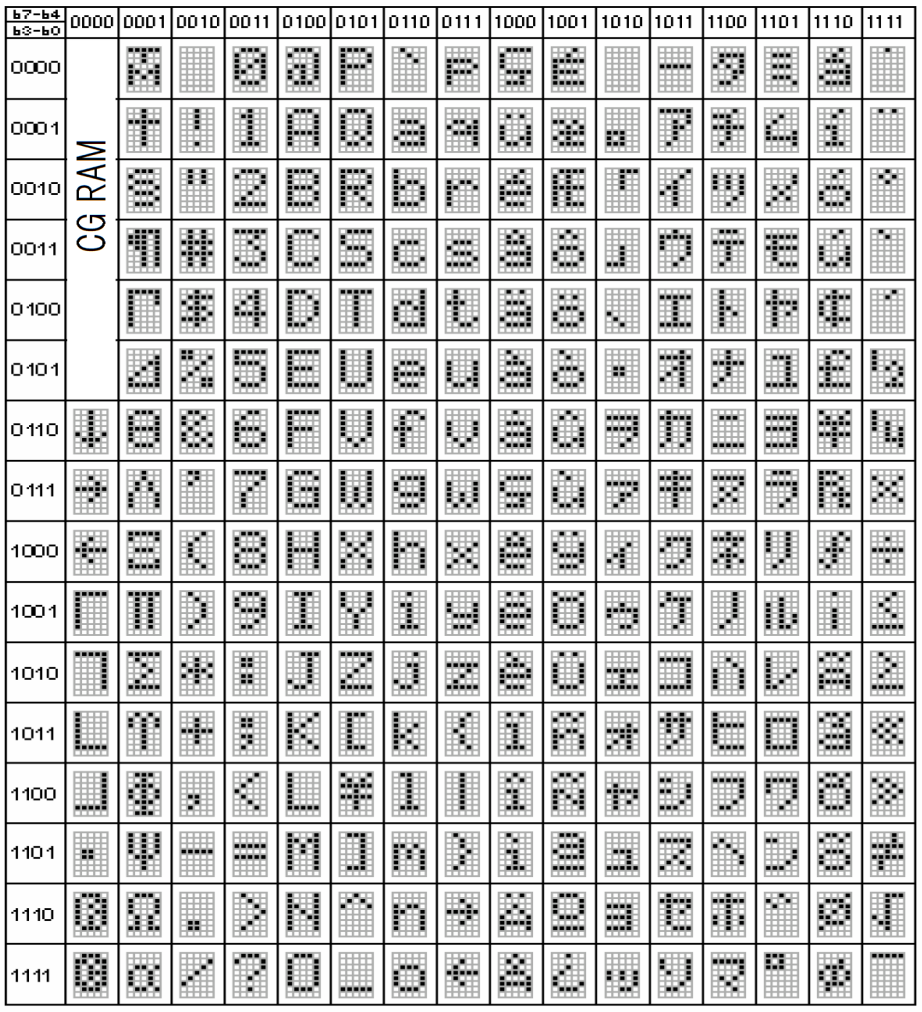
ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Typ	Max	Unit
Operating temperature	Top	-20	-	70	ºC
Storage temperature	Tst	-30	-	80	ºC
Input voltage	Vin	Vss	--	Vdd	V
Supply voltage for logic	Vdd- Vss	2.7	-	5.5	V
Supply voltage for LCD drive	Vdd- Vo	3.0	-	7.0	V

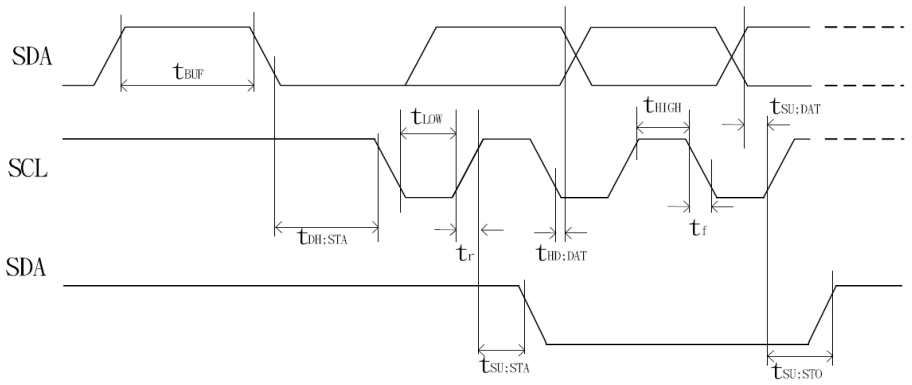
Electrical Characteristics Of LCM

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	Vdd	25ºC	3.1	3.3	3.5	V
Power Supply Current	Idd	Vdd=3.3V	--	0.5	1.0	mA
Input voltage (high)	Vih	Pins:(SDA,SCL,XRSETB),Vdd=3.3V	0.8Vdd	--	Vdd	V
Input voltage (low)	Vil		0	--	0.2Vdd	V
Recommended LC Driving Voltage	Vdd -Vo	-20ºC	4.6	4.8	5.0	V
		25ºC	4.3	4.5	4.7	
		70ºC	4.0	4.2	4.4	

CHARACTER PATTERNS



● I2C interface TIMING CHARACTERISTICS



(Ta =-30°C to 85°C)

Item	Signal	Symbol	Condition	VDD=2.7 to 4.5V Rating		VDD=4.5 to 5.5V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SI	$t_{SU;DAT}$	—	**180**	–	100	–	ns
Data hold time		$t_{HD;DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SI	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

DISPLAY INSTRUCTION TABLE

Instruction	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	OSC=380KHz	OSC=540kHz	OSC=700KHz
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC	1.08 ms	0.76 ms	0.59 ms
Return Home	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.08 ms	0.76 ms	0.59 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies display shift. These operations are performed during data write and read.	26.3 us	18.5 us	14.3 us
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	D=1:entire display on C=1:cursor on B=1:cursor position on	26.3 us	18.5 us	14.3 us
Function Set	0	0	0	0	1	DL	N	DH	*0	IS	DL: interface data is 8/4 bits N: number of line is 2/1 DH: double height font IS: instruction table select	26.3 us	18.5 us	14.3 us
Set DDRAM address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	26.3 us	18.5 us	14.3 us
Read Busy flag and address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0	0	0
Write data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM/ICONRAM)	26.3 us	18.5 us	14.3 us

Note * : this bit is for test command , and must always set to "0"

Instruction table 0(IS=0)

Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	x	x	S/C and R/L: Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	26.3 us	18.5 us	14.3 us
Set CGRAM	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter	26.3 us	18.5 us	14.3 us

Instruction table 1(IS=1)

Internal OSC frequency	0	0	0	0	0	1	BS	F2	F1	F0	BS=1:1/4 bias BS=0:1/5 bias F2~0: adjust internal OSC frequency for FR frequency.	26.3 us	18.5 us	14.3 us
Set ICON address	0	0	0	1	0	0	AC3	AC2	AC1	AC0	Set ICON address in address counter.	26.3 us	18.5 us	14.3 us
Power/ICON control/Contrast set	0	0	0	1	0	1	Ion	Bon	C5	C4	Ion: ICON display on/off Bon: set booster circuit on/off C5,C4: Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us
Follower control	0	0	0	1	1	0	Fon	Rab2	Rab1	Rab0	Fon: set follower circuit on/off Rab2~0: select follower amplified ratio.	26.3 us	18.5 us	14.3 us
Contrast set	0	0	0	1	1	1	C3	C2	C1	C0	Contrast set for internal follower mode.	26.3 us	18.5 us	14.3 us

■データとコマンドのＷＲＩＴＥ方法■

ＬＣＤに対しては、書き込み（ＷＲＩＴＥ）のみが出来ます。読み込み（ＲＥＡＤ）は、出来ません。（Ｉ２ＣのＡＣＫはあります）。
また、Ｂｕｓｙフラグ、内部のDDRAMアドレスカウンターは、読み取ることが出来ません。

スレーブアドレスは、０ｘ７Ｃです。（アドレス0111110+0(RW)）

コントロールバイトで「データ、コマンドの指定」ＲＳと,「連続データ最終データの指定」Ｃｏを送信します。

コマンドの場合ＲＳ＝０、データはＲＳ＝１になります。

データを複数送る場合Ｃｏ＝１で、最終データはＣｏ＝１です。

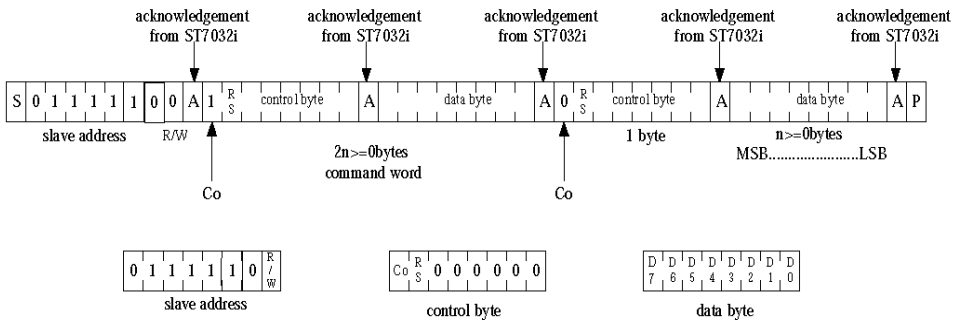


Figure 5. 2-line Interface protocol

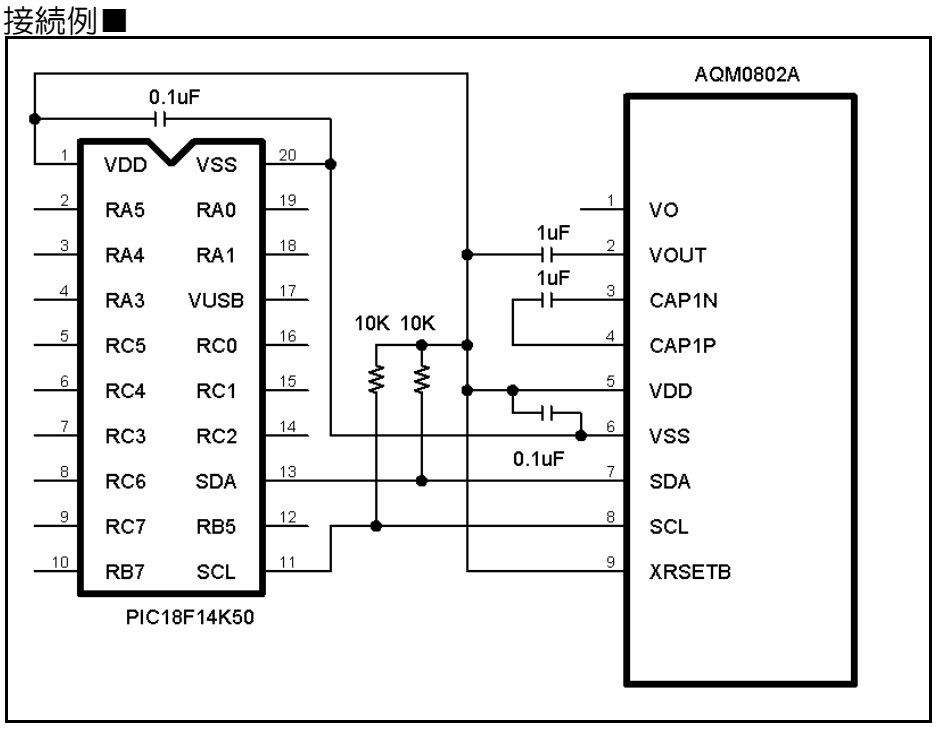
Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP condition.
	1	Another control byte will follow the data byte unless a STOP condition is received.

RS	R/W	Operation
L	L	Instruction Write operation (MPU writes Instruction code into IR)
H	L	Data Write operation (MPU writes data into DR)

■使い方■

1、基本的なコマンドは、一般的なＳＣ１６０２と同じです。
2、コントラストは、外付けＶＲではなく、拡張コマンドで設定します。
　設定前は、表示が出ません。（■の連続も出ません。）
3、コントラスト調整などの拡張コマンド（前頁 DISPLY INSTRUCTIO N TABLE のIS=1 の表）が追加されています。
　拡張コマンドを使用する場合は、「Function Set」で「IS=1」に指定します。
　拡張コマンド使用後は、「Function Set」で「IS=0」に戻します。
4、Ｉ２Ｃ端子のＳＤＡ、ＳＣＬは外部でプルアップする必要があります。
5、リセット端子ＸＲＳＥＴＢは、通常ＶＤＤに接続します。
　電源立ち上り時間などでうまくリセットされない場合は、マイコンI/Oに接続しマイコン自身のタイミングでリセットすると、良いです。
6、ＶＯＵＴ（２番ピン）、ＣＡＰ１ＮとＣＡＰ１Ｐ（３番ピンと４番ピン）には、コンデンサを付ける必要があります。
　ＶＯＵＴ　１ｕＦ　ＣＡＰ１Ｎ　ＣＡＰ１Ｐ　０．１～４．７ｕＦ
7、コントラスト調整は、拡張コマン「Power/ICONcontrol/Contras t set」のＣ５、Ｃ４と「Contrast set」のＣ３、Ｃ２、Ｃ１、Ｃ０で６４段階で設定します。
　ＶＤＤ＝３Ｖの場合、C5=1,C4=0,C3=0,C2=0,C1=0,C0=0 程度です。

■接続例■

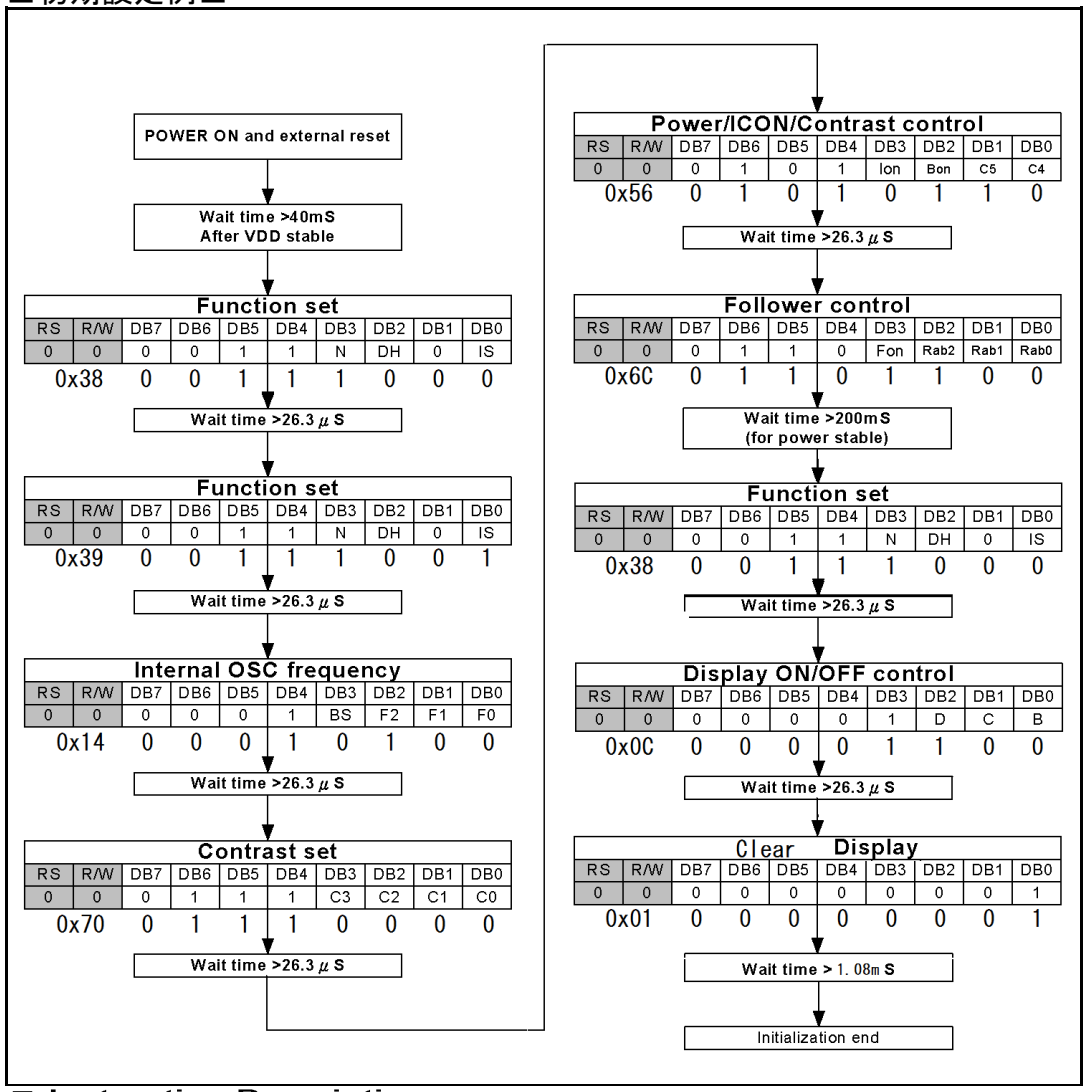


■液晶表示　DDRAMアドレス■

1行目	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07
2行目	0x40	0x41	0x42	0x43	0x44	0x45	0x46	0x47

★コントロールIC　ST7032ｉの詳しい資料は、弊社ホームページのAQM0802のページに参考pdf資料がございます。

■初期設定例■



■ Instruction Description

- **Clear Display**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

- **Return Home**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM do not change.

- **Entry Mode Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.

➢ **I/D : Increment / decrement of DDRAM address (cursor or blink)**
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when read from or write to CGRAM.

➢ **S: Shift of entire display**
When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1": shift left, I/D = "0" : shift right).

S	I/D	Description
H	H	Shift the display to the left
H	L	Shift the display to the right

- **Display ON/OFF**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

➢ **D : Display ON/OFF control bit**
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

➢ **C : Cursor ON/OFF control bit**
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

➢ **B : Cursor Blink ON/OFF control bit**
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

- **Cursor or Display Shift**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	X	X

➢ **S/C: Screen/Cursor select bit**
When S/C="High", Screen is controlled by R/L bit.
When S/C="Low", Cursor is controlled by R/L bit.

➢ **R/L: Right/Left**
When R/L="High", set direction to right.
When R/L="Low", set direction to left.

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

S/C	R/L	Description	AC Value
L	L	Shift cursor to the left	AC=AC-1
L	H	Shift cursor to the right	AC=AC+1
H	L	Shift display to the left. Cursor follows the display shift	AC=AC
H	H	Shift display to the right. Cursor follows the display shift	AC=AC

- **Function Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	DH	0	IS

➢ **DL : Interface data length control bit**
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
When in 4-bit bus mode, it needs to transfer 4-bit data by two times.

➢ **N : Display line number control bit**
When N = "High", 2-line display mode is set.
When N = "Low", it means 1-line display mode.

➢ **DH : Double height font type control bit**
When DH = " High " and N= "Low", display font is selected to double height mode(5x16 dot),RAM address can only use 00H~27H.
When DH= "High" and N= "High", it is forbidden.
When DH = " Low ", display font is normal (5x8 dot).

➢ **IS : normal/extension instruction select**
When IS=" High", extension instruction be selected (refer extension instruction table)
When IS=" Low", normal instruction be selected (refer normal instruction table)