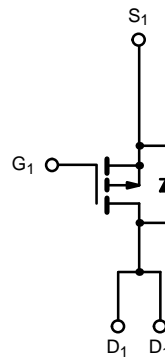
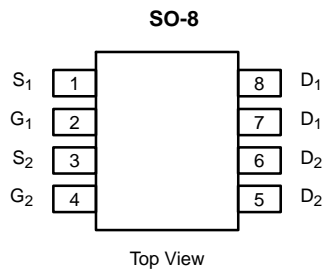
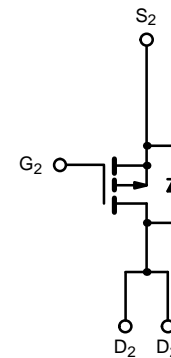


## Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
-20	0.075 @ $V_{GS} = -4.5$ V	$\pm 3.4$
	0.105 @ $V_{GS} = -3.0$ V	$\pm 2.9$
	0.115 @ $V_{GS} = -2.7$ V	$\pm 2.6$



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$	$\pm 16$	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	-2.0	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	62.5	$^\circ\text{C/W}$

Notes

 a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

 For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

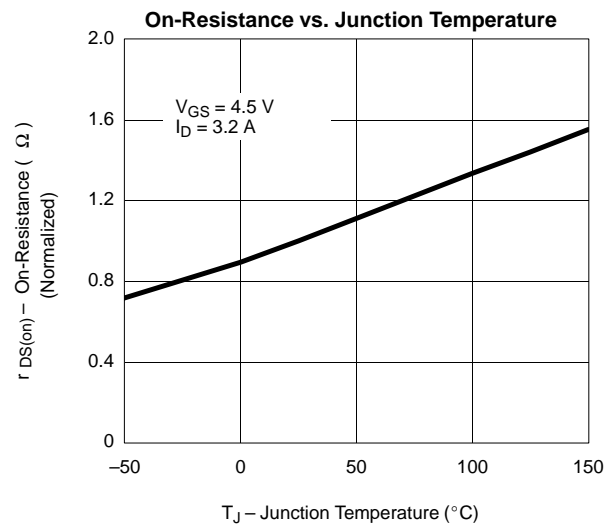
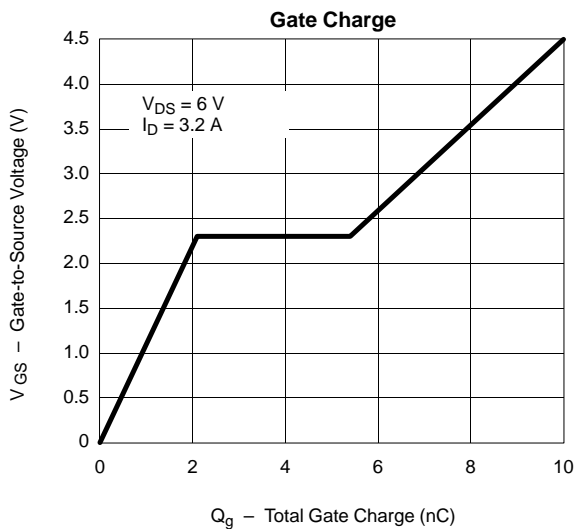
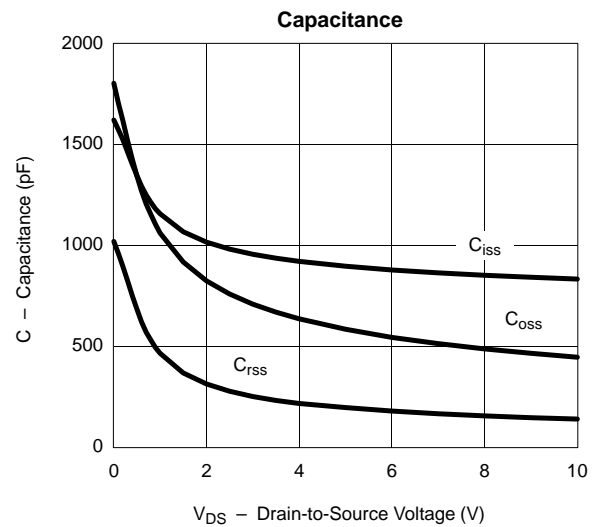
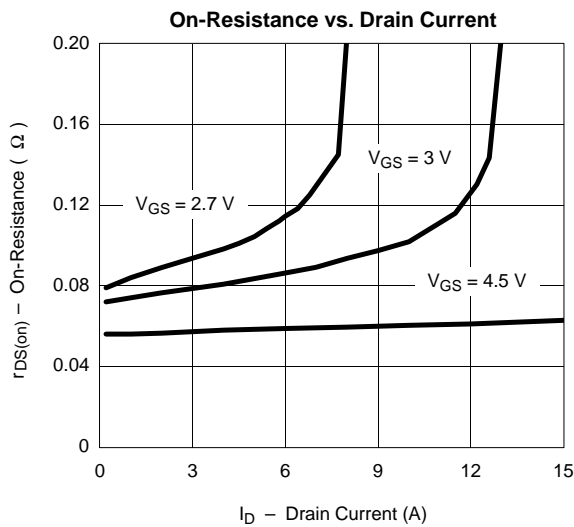
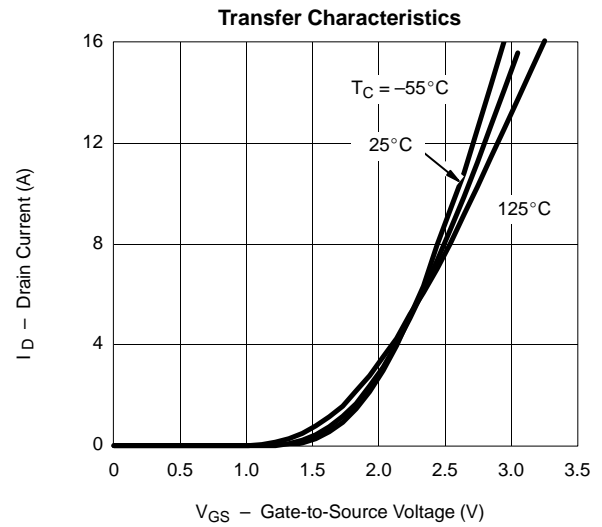
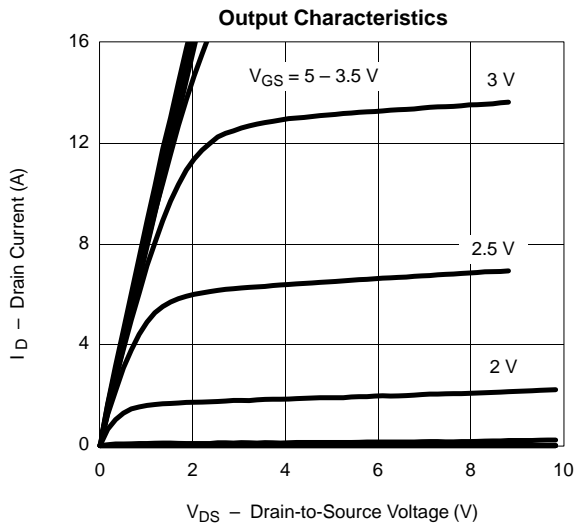
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.8			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V			-1	μA
		V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			-3	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	-16			A
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -2.7 V	-3			
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.2 A		0.06	0.075	Ω
		V <sub>GS</sub> = -3.0 V, I <sub>D</sub> = -2.0 A		0.078	0.105	
		V <sub>GS</sub> = -2.7 V, I <sub>D</sub> = -1 A		0.085	0.115	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -9 V, I <sub>D</sub> = -3.4 A		8		S
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = -2.0 A, V <sub>GS</sub> = 0 V		-0.7	-1.2	V
<b>Dynamic<sup>a</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -3.2 A		10	20	nC
Gate-Source Charge	Q <sub>gs</sub>			2.1		
Gate-Drain Charge	Q <sub>gd</sub>			3.3		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -6 V, R <sub>L</sub> = 6 Ω I <sub>D</sub> ≅ -1 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω		16	40	ns
Rise Time	t <sub>r</sub>			46	80	
Turn-Off Delay Time	t <sub>d(off)</sub>			40	70	
Fall Time	t <sub>f</sub>			25	40	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -2.0 A, di/dt = 100 A/μs		60	100	

Notes

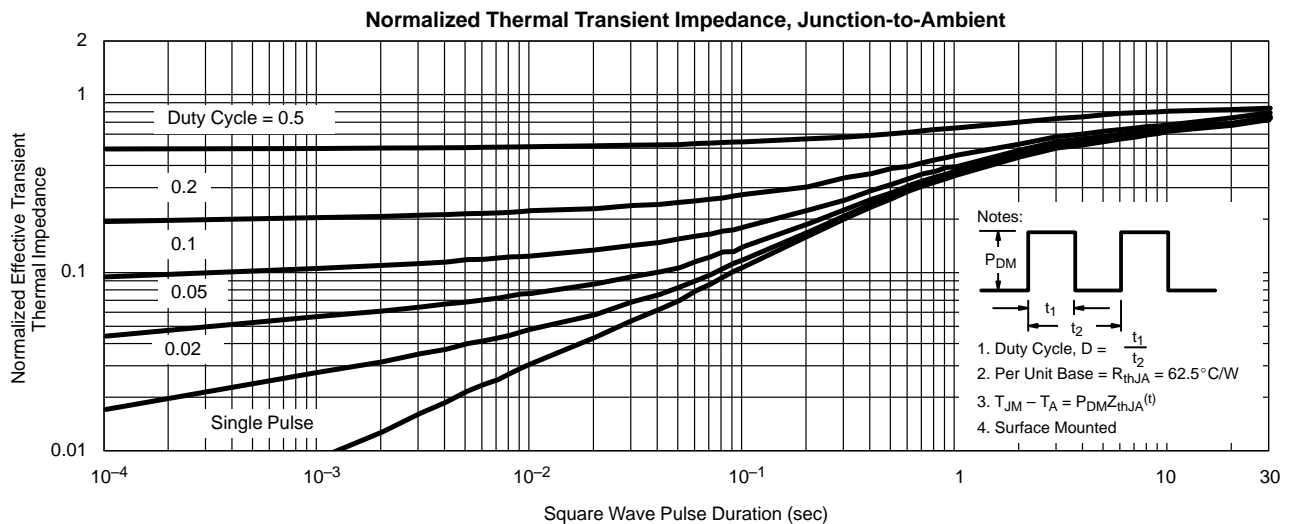
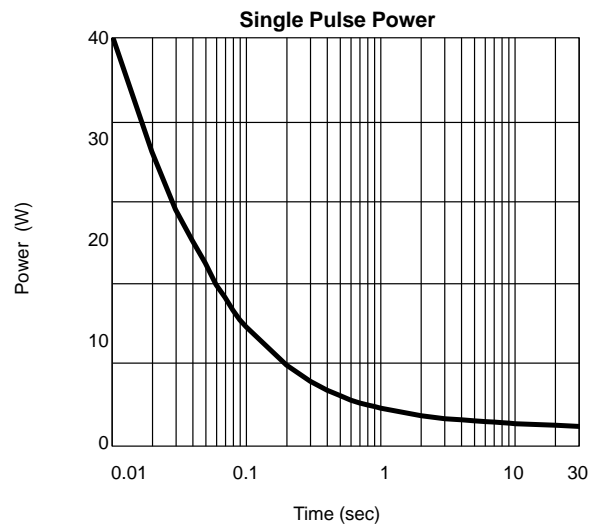
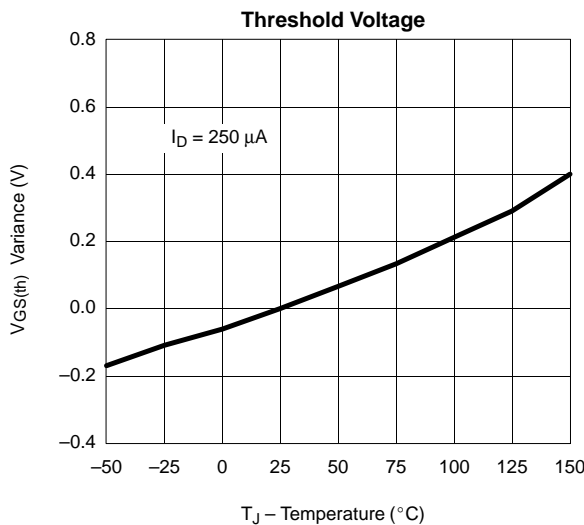
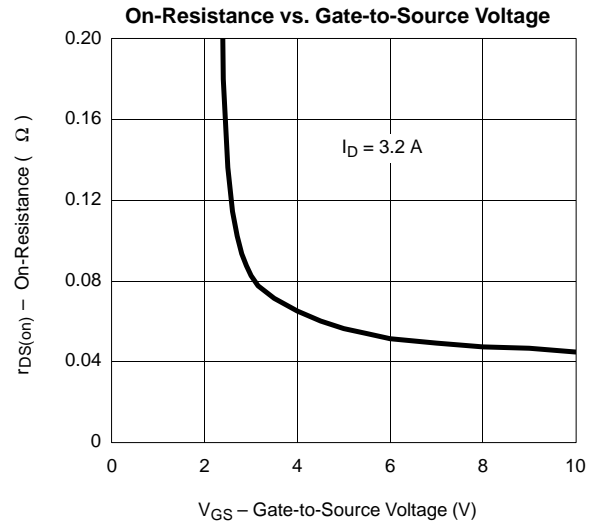
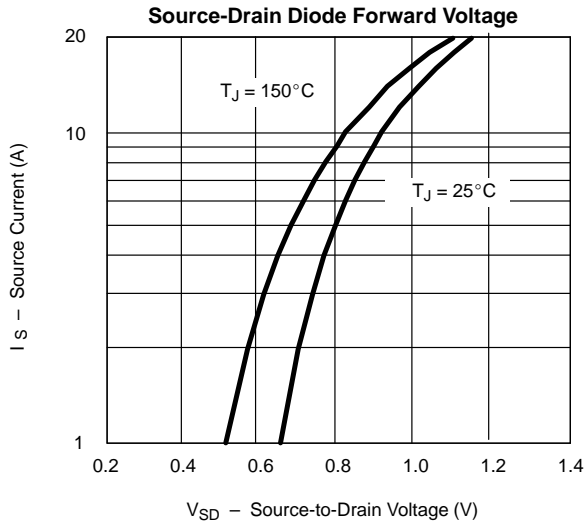
- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

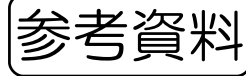


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**





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